UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/723,474	11/26/2003	Suan Jeung Boon	303.601US2	7644

21186 7590 04/23/2007

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
P.O. BOX 2938
MINNEAPOLIS, MN 55402

EXAMINER	
NGUYEN, DILINH P	
ART UNIT	PAPER NUMBER
2814	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/723,474	BOON, SUAN JEUNG	
	Examiner	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-24 and 51-88* is/are pending in the application.

4a) Of the above claim(s) *62-87* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19-24,51-61 and 88* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *1/22/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 19 and 21-24, 51-54, 56-58, 60-61 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie (U.S. Pat. 5898858) in view of Capote et al. (U.S. Pat. 6121689) and Gilleo (U.S. Pat. 6265776).

Gillespie discloses an electronic system comprising:

a processor and a memory controller are integrated into a BGA chip package (fig. 3, abstract).

Gillespie does not explicitly disclose the chip package includes an adhesive layer covering the chip and having an array of column-shaped openings aligned with connection pads having a chamfer opposite the first surface of the adhesive layer at each of the openings and a conductive a conductive material substantially filling the array of openings.

However, Capote et al. disclose a flip chip includes:

a first semiconductor device 10 having a first side and a second side, the first side comprising a first array of connection pads 24, the connection pads electrically coupled to circuits on the first semiconductor device;

an adhesive layer 22 covering the first side of the first semiconductor device with a first surface of the adhesive layer contacting the first side, the adhesive layer having an array of column-shaped openings 28 (figs. 6 and 7) substantially aligned with one or more connection pads of the first array of connection pads; and

a conductive material 30 substantially filling the array of openings (figs. 3, 6-7, column 7, lines 60 et seq.) in order to provide a flip chip configuration.

Gilleo discloses a semiconductor device comprising a wafer 12; an underfill layer 18 covering the first side of the wafer 12 with a first surface of the underfill layer contacting the first side and having a chamfer, opposite the first surface of the underfill layer 18 (cover fig.) in order to form the contact angles at the interface between the flux coating and the underfill layer (column 8, lines 2-3).

Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to have an adhesive layer covering the chip and having an array of openings aligned with connection pads having a chamfer and a conductive material substantially filling the array of openings as taught by Capote et al. and Gilleo into the device of Gillespie in order to provide a flip chip configuration without bending the chip and substrate and form the contact angles at the interface between the flux coating and the underfill layer.

- Regarding claim 21, Capote et al. disclose that the adhesive layer 22 is comprised of film layer (fig. 3, column 8, lines 12-18).
- Regarding claim 22, Capote et al. disclose that the adhesive layer includes a curable, fluid material (fig. 3, column 8, lines 17-18).

- Regarding claim 23, Capote et al. disclose that the conductive material is solder 30 (fig. 7, column 9, lines 3).
- Regarding claim 24, Capote et al. disclose that the conductive material is cylindrical in shape (fig. 7).
- Regarding claim 52, Capote et al. disclose that the adhesive layer includes a thermoplastic material (column 22, lines 16-17).
- Regarding claims 51-53, Gilleo discloses that the underfill layer 18 includes a thermoplastic material or thermoset material (column 4, lines 30-32) and the underfill layer 18 would includes an elastomer.
- Regarding claim 54, Capote et al. discloses that the adhesive layer 22 is applied to the chip in either liquid or adhesive tape form; therefore, the adhesive layer includes a pressure-sensitive material (column 8, lines 17-18).
- Regarding claim 56, Capote et al. disclose that the conductive material includes a conductive paste (column 3, lines 54-55) that hardens upon curing.
- Regarding claim 57, Capote et al. disclose that the conductive material includes a conductive that hardens upon curing and it would have been obvious to one having ordinary skill in the art to have the conductive material includes a conductive gel.
- Regarding claim 58, Capote et al. discloses that the conductive material 30 is column-shaped (fig. 7).

- Regarding claim 60, Capote et al. disclose that the conductive material 30 is flush with a surface of the adhesive layer 22 opposite the first surface of the adhesive layer (fig. 8).
- Regarding claim 61, Capote et al. disclose that the conductive material 30 protrudes beyond a surface of the adhesive layer 22 (fig. 7).
- Regarding claim 88, Capote et al. disclose that the conductive material 30 and the adhesive layer 22 are free from an underfill (fig. 6).

3. Claims 20, 55 and 59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gillespie (U.S. Pat. 5898858) in view of Capote et al. (U.S. Pat. 6121689) and Gilleo (U.S. Pat. 6265776) as applied to claim 19 above, and further in view of Toyosawa et al. (U.S. Pat. 6337257).

Gillespie, Capote et al. and Gilleo substantially disclose all the limitations as claimed above except for a protective material substantially covering the second side of the semiconductor device.

However, Toyosawa et al. disclose a semiconductor package comprising a second surface 36 of a semiconductor chip 32 are in contact with a protective tape (cover fig., column 12, lines 28-30). Therefore, it would have been obvious to one having ordinary in the art at the time the invention was made to modify the device structure of the above combination by having a protective material covering the second side of the semiconductor device because as taught by Toyosawa et al., such protective material would protect and reinforce the back surface of the semiconductor chip for use in a semiconductor package (column 12, lines 28-30).

- Regarding claim 55, it would have been obvious to form the protective coating or the protective tape includes an epoxy.
- Regarding claim 59, Toyosawa et al. disclose the second side of the first semiconductor device includes a bonding layer (column 12, lines 28-30).

Response to Arguments

Applicant's arguments filed 1/22/07 have been fully considered but they are not persuasive.

- Applicant argues that Capote et al. fail to teach or suggest a conductive material filling the array of column-shaped openings.

Applicant's argument has been fully considered but it is not persuasive because Capote et al. clearly disclose a conductive material 30 filling the array of column-shaped openings 28 (figs. 6-7).

- Applicant argues that Capote et al. do not disclose an adhesive layer covering the chip and having an array of column-shaped openings with a chamfer, and a conductive material filling the array of column-shaped openings, opening having a chamfer.

Applicant's arguments have been fully considered but they are not persuasive because this argument has no immediate apparent relevance to the issues presented by the rejection before us since an appellant cannot show nonobviousness by attacking references individually wherein the rejection is based upon a combination of references. In re Young, 403 F. 2d 754, 757, 159 USPQ 725, 728 (CCPA 1968).

It should be noted that the rejection of claims 19 and 21-24, 51-54, 56-58, 60-61 and 88 are not based on anticipation, but rather, are based on obviousness.

Examiner relies on the combined teachings at Gillespie, Capote et al. and Gilleo. Capote et al. is relied on for teaching the adhesive layer covering the chip and having an array of column-shaped openings, and a conductive material filling the array of column-shaped openings but not relied on for teaching the openings with chamfer. The Examiner thus regards the Applicant's assertions as constituting evidence that the Applicant has failed to consider as a whole the prior art teachings disclosed by the combining of the references.

- In response to applicant's argument that there is improper to combine the references, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 5:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DLN

HOAI PHAM
PRIMARY EXAMINER